**module ucounter\_3b (clk, reset, out);**

**input clk, reset;**

**output [2:0] out;**

**reg [2:0] out;**

**always @ (reset or negedge clk)**

**if (reset)**

**out = 3'b000;**

**else**

**out = out + 1;**

**endmodule**

**module test\_ucounter\_3b;**

**reg clk, reset;**

**wire [2:0] out;**

**ucounter\_3b dut (clk, reset, out);**

**initial begin**

**reset = 1;**

**clk = 0;**

**#50**

**reset = 0;**

**end**

**always**

**#30 clk = ~clk;**

**endmodule**